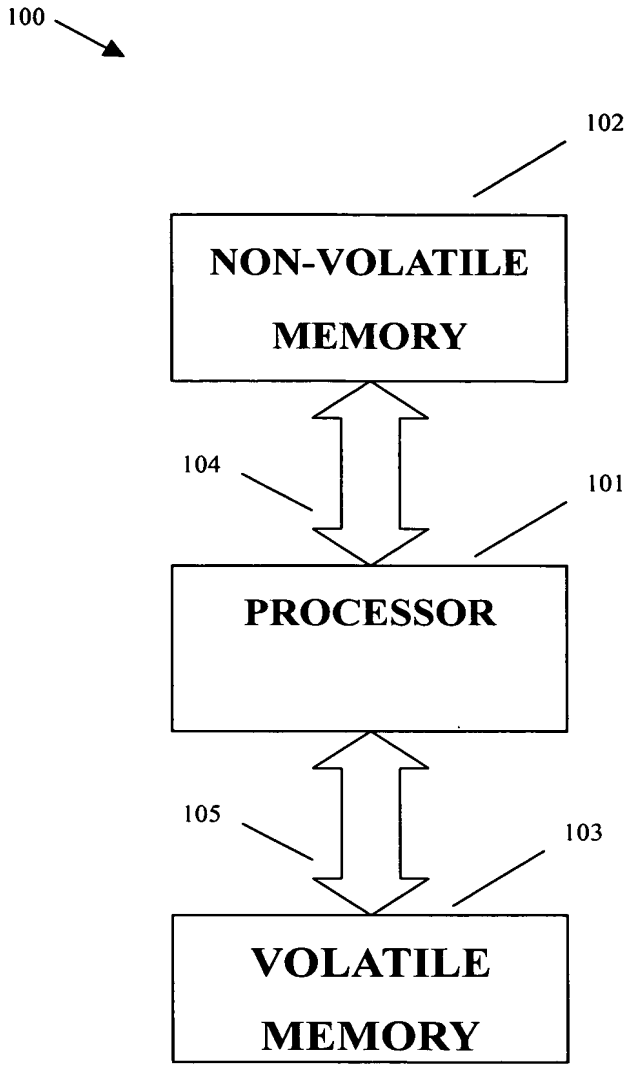
100
102
NON-VOLATILE MEMORY
104
101
PROCESSOR
105
103
VOLATILE MEMORY

FIG. 1

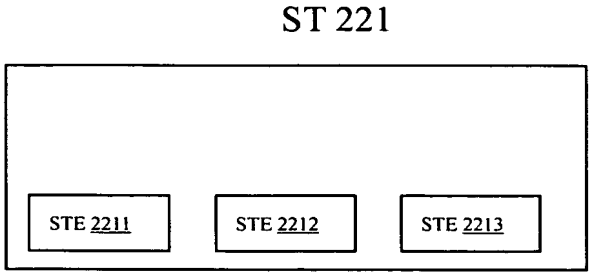

FIG. 3

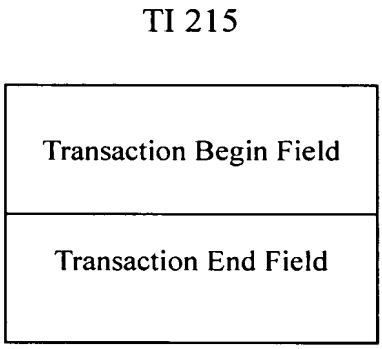

FIG. 4a

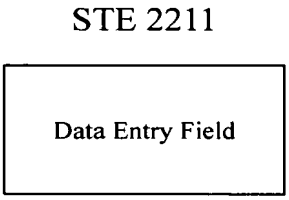

FIG. 4b

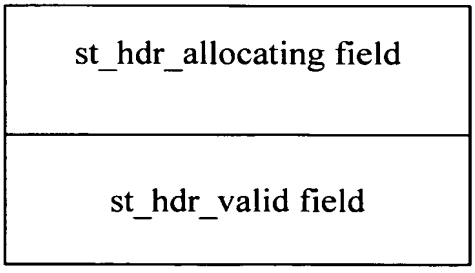

FIG. 4c

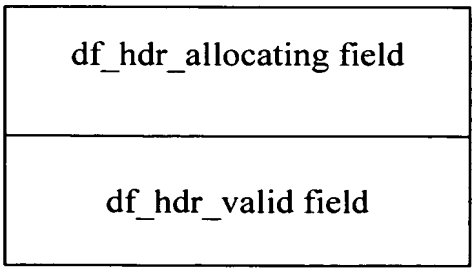

FIG. 4d

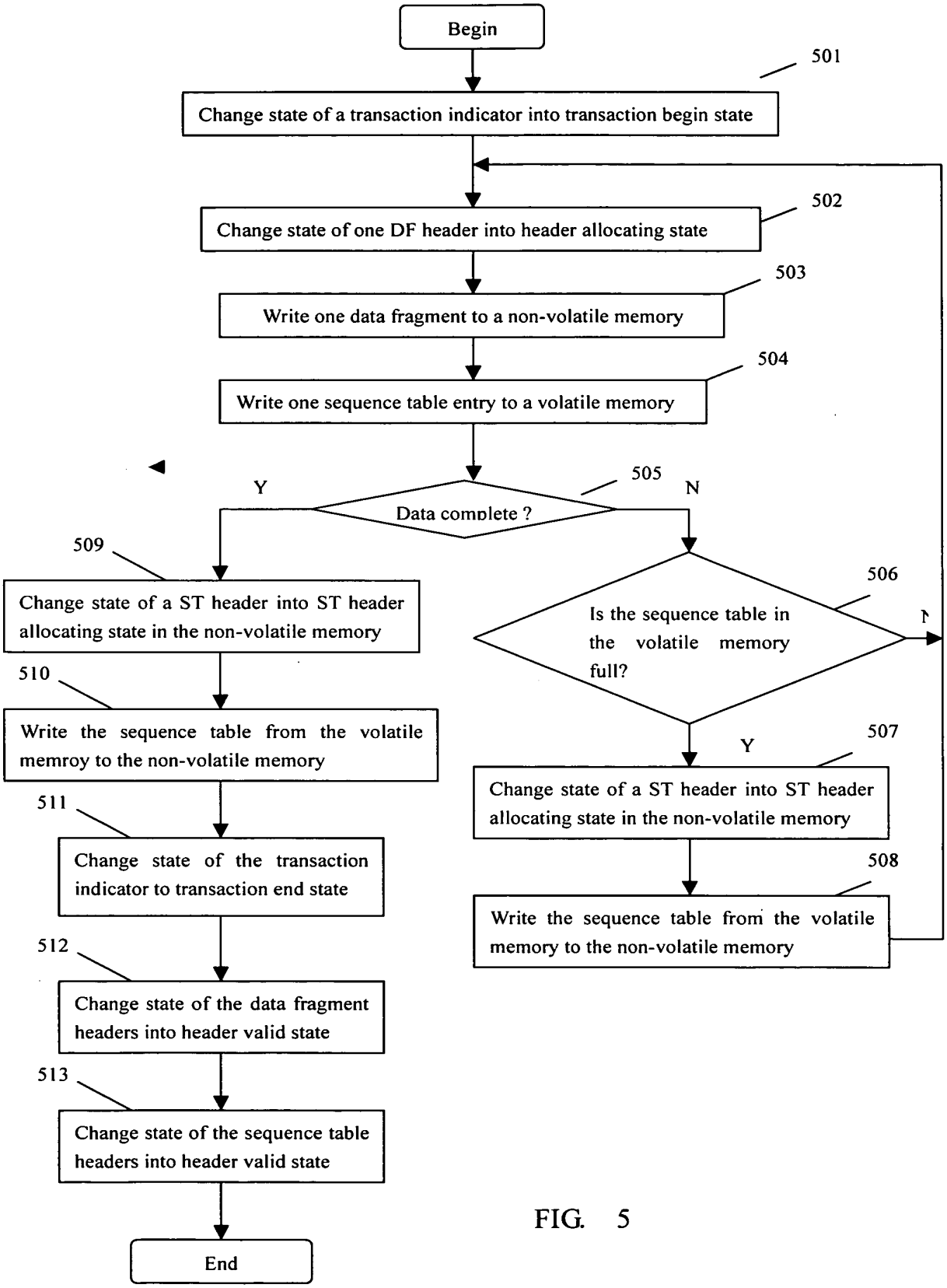
Begin
501
Change state of a transaction indicator into transaction begin state
502
Change state of one DF header into header allocating state
503
Write one data fragment to a non-volatile memory
504
Write one sequence table entry to a volatile memory
505
Data complete ?
Y
N
509
Change state of a ST header into ST header allocating state in the non-volatile memory
510
Write the sequence table from the volatile memroy to the non-volatile memory
511
Change state of the transaction indicator to transaction end state
512
Change state of the data fragment headers into header valid state
513
Change state of the sequence table headers into header valid state
End
506
Is the sequence table in the volatile memory full?
Y
507
Change state of a ST header into ST header allocating state in the non-volatile memory
508
Write the sequence table from the volatile memory to the non-volatile memory

FIG. 5

	Sequence Table	Data Fragment	Write Mode
1		hdr_allocating (1)	1 Bit Twiddling
2		Data Fragment (1)	1 KB Buffer Programming
3	hdr_allocating		1 Bit Twiddling
4	entry_allocating (1)		1 Bit Twiddling
5	data entry (1)		2 Words Programming
6	entry_valid (1)		1 Bit Twiddling
7		hdr_valid (1)	1 Bit Twiddling
8	...	...	...
9		hdr_allocating (64)	1 Bit Twiddling
10		Data Fragment (64)	1 KB Buffer Programming
11	entry_allocating (64)		1 Bit Twiddling
12	data entry (64)		2 Words Programming
13	entry_valid (64)		1 Bit Twiddling
14	hdr_valid		1 Bit Twiddling
15		hdr_valid (64)	1 Bit Twiddling

Bit twiddling (bits)	258
word program (words)	128
Buffer program (bytes)	64K

	Sequence Table	Data Fragment	Write Mode
1	transaction begin		1 Bit Twiddling
2		hdr_allocating (1)	1 Bit Twiddling
3		Data Fragment (1)	1 KB Buffer Programming
4		...	...
5		hdr_allocating (64)	1 Bit Twiddling
6		Data Fragment (64)	1 KB Buffer Programming
7	hdr_allocating		1 Bit Twiddling
8	data entries		0.5KB Buffer Programming
9	transaction end		1 Bit Twiddling
10		hdr_valid (1)	1 Bit Twiddling
11		...	...
12		hdr_valid (64)	1 Bit Twiddling
13	hdr_valid		1 Bit Twiddling
14			

Bit twiddling (bits)	132
word program (words)	0
Buffer program (bytes)	64.5K

Fig. 6

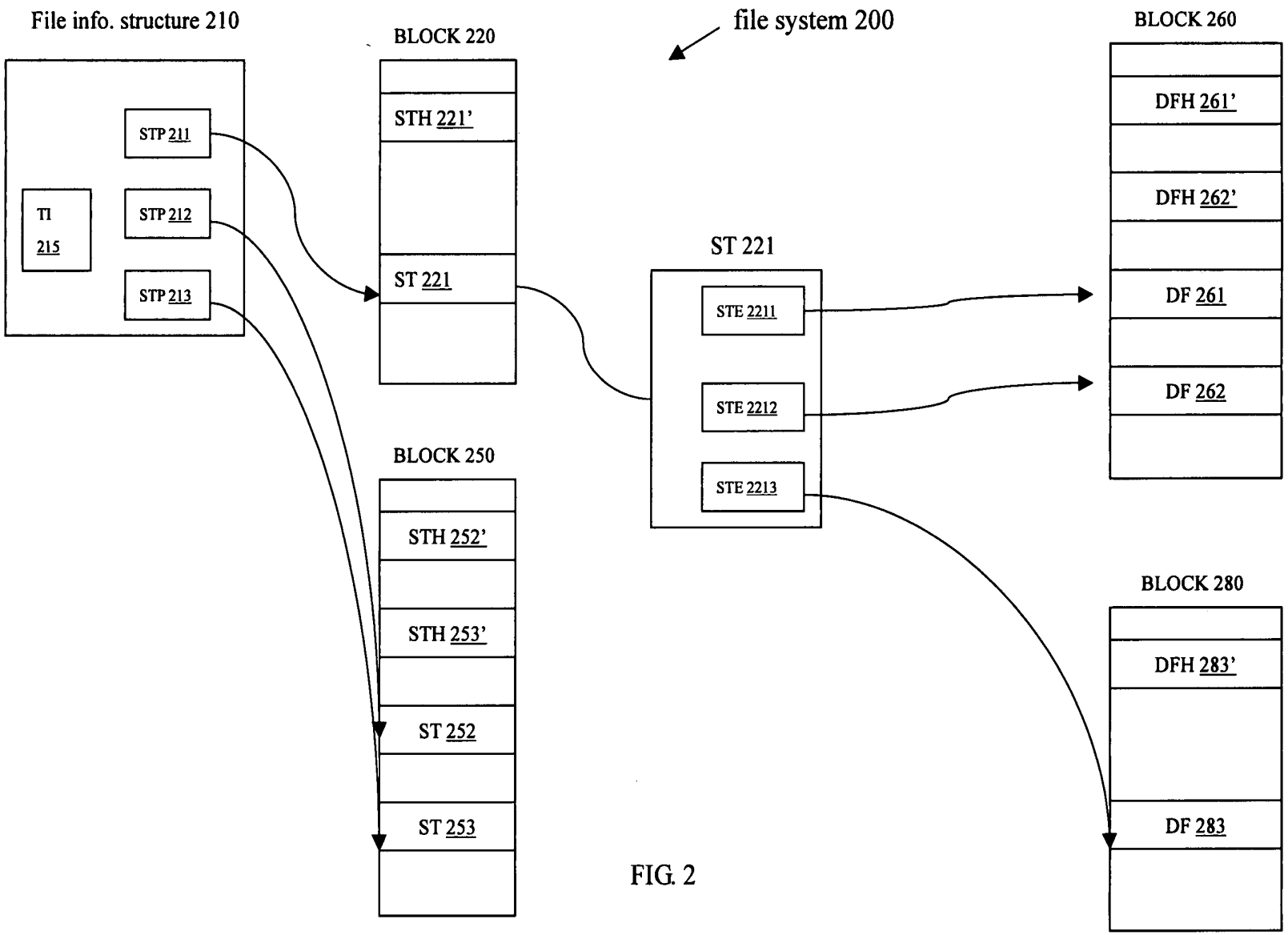
File info. structure 210
STP 211
TI 215
STP 212
STP 213
BLOCK 220
STH 221'
ST 221
BLOCK 250
STH 252'
STH 253'
ST 252
ST 253
file system 200
ST 221
STE 2211
STE 2212
STE 2213
BLOCK 260
DFH 261'
DFH 262'
DF 261
DF 262
BLOCK 280
DFH 283'
DF 283

FIG. 2